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Multilayer buffer system for fabrication of high-T_c edge-geometry SNS weak links on silicon-on-sapphire substrates

B. D. Hunt, M. C. Foote, W. T. Pike, J. B. Barner, and R. P. Vasquez

Center for Space Microelectronics Technology, Jet Propulsion Laboratory,
California Institute of Technology, Pasadena, CA 91109

ABSTRACT

High frequency detector and circuit applications often require device fabrication on medium-to-low-dielectric constant substrates ($\varepsilon < 12$), Silicon-on-sapphire (SOS) substrates have acceptably low dielectric constants and provide other important advantages, including the possibility of monolithic integration of silicon and superconducting circuitry. Our initial results with $YBa_2Cu_3O_{7-x}$ (YBCO) edge-geometry superconductor/normal-metal/superconductor (SNS) weak links fabricated on r-plane SOS substrates using cubic zirconia (YSZ) buffer layers revealed problems with grain boundary nucleation in the YBCO counterelectrode. These results motivated development of a new multilayer buffer system consisting of an epitaxial YSZ film grown on an SOS substrate, overlayed by a thin YBCO "seed" layer, and an epitaxial $SrTiO_3$ (STO) layer. STO - YBCO bilayers grown over the YBCO seed layer show a remarkable improvement in epitaxial quality and in YBCO electrical properties relative to similar bilayers grown directly on the YSZ buffer. In addition, SNS weak links fabricated on SOS substrates using the multilayer buffer system exhibit dramatically improved electrical characteristics compared to devices produced on YSZ buffer layers. These are the first epitaxial edge-geometry SNS weak links produced on SOS substrates.

1. INTRODLJCTION

Excellent progress has been made over the past several years in the development of IITS Josephson weak links utilizing a number of different device technologies. One of the most promising approaches is an epitaxial edge-geometry SNS device structure using an oxide normal metal deposited on an ion-milled YBCO base electrode edge[1,2,3,4,5,6]. While much room for device optimization remains, these HTS weak links are approaching the quality needed for a variety of high frequency applications including Josephson mixers for sub-mm wave receivers, local oscillators for mixers, and ultra-high speed logic circuits. Such high frequency applications will require low-to-medium dielectric constant substrates ($\varepsilon \leq 12$) in order to maximize coupling to the active elements and to maximize the propagation velocity in circuit interconnects. An additional influence on substrate choice is the fact that many applications would also benefit from the ability to integrate silicon and superconductor circuitry on the same substrate. However, acceptable substrates for HIS film growth arc limited by the requirements for a reasonable lattice match to the oxide superconductor, as well as chemical compatibility with the superconductor at typical growth temperatures. In part because of these constraints, most HTS film growth and device Studies have been done on much higher-dielectric-constant substrates, such as $LaAlO_3$ ($\varepsilon \approx 25$) or $SrTiO_3$ ($E = 300$).

Recent progress in buffer layer technology has relaxed some of the limitations on substrate selection, and made new substrate choices possible. A number of groups have demonstrated that high quality epitaxial YBCO films can be grown on YSZ and other buffer layers on Si[7,8,9,10,11,12] anti Si-on-sapphire (SOS) substrates [13,14]. These substrates are attractive for high frequency applications because they have moderate dielectric constants ($\varepsilon_{Si} \approx 12$, $\varepsilon_{SOS} \approx 9$-11) and allow for the possibility of Si device integration. However, YBCO films grown on Si suffer from cracking and aging problems in layers thicker than about 500 Å due to the thermal expansion mismatch between YBCO and Si[8,11]. Silicon-on-

sapphire is a better substrate for HTS high-frequency device fabrication for a variety of reasons. Sapphire has a thermal expansion coefficient more closely matched to YBCO, and YBCO films as thick as 4000 Å can be grown on SOS substrates without cracking [13]. SOS substrates are also robust and have low high-frequency losses. In addition, silicon-on-sapphire growth technology is well-enough developed that SOS wafers with CMOS-quality Si are commercially available. Most research to date has focused on optimization of single-layer YBCO film growth on various buffer layers on SOS substrates, but Bums et al. have recently reported the fabrication of HTS grain-boundary junctions and flux-flow transistors combined with small-scale CMOS circuits on the same SOS chip [15].

However, to our knowledge, there have been no reports of epitaxial SNS edge-geometry weak links on any moderate-dielectric-constant substrates, including Si and SOS. This may be due in part to the fact that the fabrication of edge-geometry weak links puts additional restrictions on the choice of substrate and associated buffer layers, because good epitaxy must be maintained across the interface between the YBCO base electrode and the underlying material. Such a requirement is nontrivial because some of the commonly-used buffer layers form interracial reaction layers with YBCO, and are not lattice-matched to YBCO in the c-axis. These points will be discussed in more detail below. This paper examines a new buffer layer scheme for YBCO film growth on SOS substrates, which is compatible with epitaxial edge-geometry weak link fabrication. Results on the fabrication of SNS weak links on this multilayer buffer system are described and contrasted to results for weak links on single YSZ buffer layers. In addition to the focus on epitaxial SNS devices, the present study differs from previous HTS device work on SOS substrates in that the HTS weak links are produced directly over buffer layers on the underlying Si epilayer, rather than on a portion of the substrate where the Si has been etched a way [15]. This approach allows, in principal, three-dimensional integration of Si and HTS circuits, as well as superconducting interconnect runs above underlying Si circuitry, although nonepitaxial portions of the Si circuit (e.g. the MOS gates) would have to be avoided.

2. EDGE-GEOMETRY SNS WEAK LINK FABRICATION

The basic device structure used in this work is an edge-geometry SNS weak link, as shown in Figure 1. The device consists of a c-axis-oriented YBCO base electrode with an exposed edge. An epitaxial normal metal is deposited on the YBCO edge, followed by deposition of the YBCO counterelectrode. Because the top surface of the base electrode is covered by a thick insulator, electrical contact between the YBCO electrodes is confined to the edge of the lower YBCO film, The edge geometry has a number of important advantages, including the facts that: 1) the critical N/S interfaces are located on the longer-coherence-length YBCO surfaces; 2) precisely-controlled, very short bridge lengths are achievable; 3) submicron device areas can be realized using conventional photolithography; and 4) the counterelectrode serves as the wiring layer, which simplifies circuit fabrication.

Details of the film deposition and edge-geometry weak link fabrication processes have been described previously [2,5,16,17,18], but will be briefly summarized here, including some recent process changes made to improve YBCO film quality and device yield. Device fabrication begins with pulsed laser deposition (PLD) of a c-axis-oriented YBCO thin film onto a substrate or previously deposited buffer layers. The PLD process is generally done at a target-to-substrate distance of 5 cm, with the laser beam scanned radially over a rotating 2 inch diameter target. Our recent device work has utilized ablation targets of nominal composition $YBa_{1.95}La_{0.05}Cu_3O_{7-x}$, because a small amount of La doping results in higher transition temperatures [19]. Following growth of the base electrode, a thin (100-300 Å), nonepitaxial MgO, YSZ, or $SrTiO_3$ passivation layer is deposited over the YBCO before removal from the laser ablation chamber. Next a thick (≈ 0.4 to 0.8 μm) MgO, YSZ, or $SrTiO_3$ layer is patterned using a chlorobenzene or reversal-process photoresist liftoff stencil. The patterned insulator film is utilized as an ion milling mask with 300-500 CV Ar ions at a milling angle of 60° from the substrate

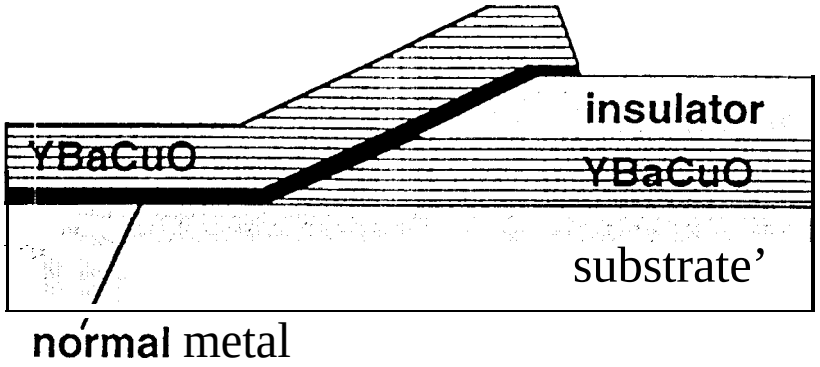

Figure 1. Schematic cross-sectional diagram of an edge-geometry YBCO/normal-metal/YBCO SNS weak link with c-axis-oriented YBCO thin films.

normal to produce a tapered edge in the YBCO base electrode. The edge cutting step is sometimes followed by a low energy (50eV) ion cleaning step. Just after milling of the YBCO edge, within the same vacuum system, the normal metal layer and YBCO counterelectrode are deposited at the appropriate growth temperatures (≈ 775-815 C for YBCO). A lithography-ion milling step is then used to pattern via holes down to the base YBCO film and liftoff Au contact pads. Finally, another lithography-milling process defines the counterelectrode. Completed devices have counterelectrode widths ranging from 25 μm to 1.25 μm.

It is important to note that the edge-cutting process inevitably mills at least partially into the substrate or buffer layers below the YBCO base electrode edge. As a result, the normal metal and counterelectrode must grow over the base-electrode/substrate (or buffer layer) interface. If the c-axis lattice constant of the substrate or buffer layer does not match that of YBCO, or a YBCO-substrate (buffer layer) reaction layer exists, epitaxial growth of the normal metal and counterelectrode may be disrupted, resulting in formation of a grain boundary in these layers. Propagation of the grain boundary up through the counterelectrode would result in creation of a grain boundary weak link, which would appear in series with the SNS weak link at the base electrode edge. Thus it is important to use substrates and buffer layers which provide a c-axis lattice match, and do not form a reaction layer at the YBCO interface. As will be seen below, this criterion rules out the use of YSZ substrates and buffer layers for edge junction fabrication. $LaAlO_3$ and $SrTiO_3$ have been successfully used for fabrication of edge-geometry weak links. Although these cubic materials do not have a c-axis lattice constant close to YBCO, their lattice constants are very close to one third of the YBCO c-axis so that an effective lattice match is still possible. A YSZ/CeO_2 buffer layer system has been shown to produce excellent quality **YBCO films** on SOS[14], but CeO_2 may not be suitable for edge junction fabrication because it does not lattice match YBCO in the c-axis (CeO_2 is cubic with a = 5.41 Å), and a YBCO-CeO_2 reaction layer is known to form for growth temperatures near 790 C[20].

3. SNS WEAK LINKS ON YSZ BUFFER I. AYERS ON SOS SUBSTRATES

Fabrication of YBCO films and devices on Si or SOS substrates requires a buffer layer to prevent reaction between YBCO and Si. The most commonly used buffer layer has been cubic zirconia, because YSZ buffer layers grown epitaxially on Si enable the growth of high quality YBCO overlayers. Following the work of Fork and coworkers, wc developed a YBCO film growth process over YSZ buffer layers on HF-cleaned SOS substrates. The r-plane $\{1\bar{1}02\}$ SOS substrates are obtained commercially[21], and come with nominally undoped, 0.3 μm thick Si epilayers. immediately following

the HF-cleaning process, the SOS substrates are mounted with tape on a Haynes metal frame with a hole slightly smaller than the 1.2 inch square substrate, and loaded into the deposition system. The substrates are radiantly heated to the growth temperature in vacuum, a small amount (≈ 10 Å) of YSZ is deposited, and then 1 mT of oxygen is admitted and the YSZ deposition is completed. The YSZ growth is followed by growth of the YBCO layer at nominally the same temperature, but a higher oxygen pressure (120-400 mT). The actual growth temperatures are not well known because of difficulties with temperature measurement associated with the radiant heating process, but are estimated to be approximately 800 C. Typical YSZ buffer layer and YBCO base electrode thicknesses are 0.2 μm and 0.15 μm, respectively, and YBCO film quality is comparable to films grown on $LaAlO_3$ substrates. Following deposition of the YBCO base electrode and the overlying passivation layer, our standard edge junction process was used to fabricate SNS weak links with 150 Å $PrBa_2Cu_3O_{7-x}$ (PBCO) normal metal layers and 1400 Å YBCO counterelectrodes. The total YBCO thicknesses were kept below 4000 Å to minimize potential problems with thermal-stress-induced cracking of the YBCO films.

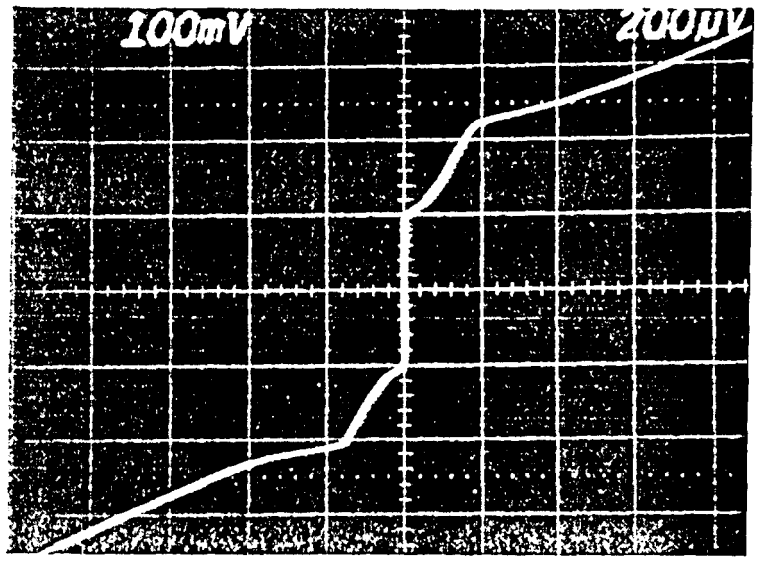

Figure 2. Current-voltage characteristics for a YBCO edge-geometry weak link on a YSZ buffer layer on an SOS substrate with a 150 Å PBCO normal metal layer at 4.2 K. The counterelectrode is 3 μm wide, and the base electrode is 1500 Å thick. The I-V curve suggests the existence of a series grain-boundary weak link. The vertical scale is 100 μA/div, and the horizontal scale is 200 μV/div.

Figure 2 shows typical current-voltage (I-V) characteristics for a YBCO SNS edge-geometry weak link on a YSZ buffer layer on silicon-on-sapphire with a 150 Å PBCO normal metal layer at 4.2 K. These electrical characteristics clearly suggest the presence of a second weak link in series with the PBCO weak link. The most likely explanation of a series weak link is the formation of a grain boundary in the YBCO counterelectrode. Such a grain boundary could nucleate at the interface between the YBCO base electrode and the YSZ buffer layer. We have used cross-sectional high-resolution transmission microscopy (HRTEM) to examine this interface in unpatterned YBCO/YSZ bilayers and found that a thin 30-50 Å reaction layer forms between the YBCO and YSZ. Other workers have also observed this reaction layer and indentified it as $BaZrO_3$, which has a cubic perovskite structure with a lattice constant of 4.2 Å[20,22,23]. A grain boundary could nucleate at the YBCO-YSZ interface either due to this lattice-mismatched reaction layer; due to the lattice mismatch in the c-axis between the PBCO and YBCO overlayers and the YSZ buffer; or due to reaction between the PBCO normal metal layer and

the YSZ buffer. We have found that the I-V characteristics of SNS weak links fabricated on YSZ buffer layers on $LaAlO_3$ also show double weak link behavior, confirming that the YSZ buffer is causing the series-weak-link problem, rather than some stress-related or other effect associated with the SOS substrates, Other recent work has also shown that YSZ substrates lead to grain boundary nucleation problems in HTS edge-geometry devices[24]. Although the exact cause of the series weak link is not known at this point, it is clear that there is a problem related to the YSZ buffer layers, and an alternate buffer layer system is needed for weak link fabrication on SOS substrates .

4. SNS WEAK LINKS ON $SrTiO_3$ BUFFER LAYERS ON SOS SUBSTRATES

4.1 YBCO/$SrTiO_3$/YSZ/SOS heterostructures

Because the base electrode YBCO-YSZ interface apparently leads to grain boundary formation in the YBCO edge junction counterelectrodes, direct contact between the YBCO base electrode and YSZ must be avoided. In principal the YSZ could be eliminated entirely by using a different buffer layer such as SrTi03 (STO), which is known to be compatible with edge-geometry weak link fabrication. STO has a relatively high dielectric constant, but this should not have a big effect for STO thicknesses much less than a wavelength at the frequencies of interest. However, it is also known that STO does not grow epitaxially on the Si (100) surface[8], so that direct growth of an STO buffer layer on SOS is not possible and another process is necessary. Because YSZ does grow well on Si(100), an obvious alternate approach is to grow STO over a YSZ buffer layer on SOS as shown in Figure 3. In a test of this method, wc used pulsed-laser deposition to grow YBCO/STO/YSZ heterostructures on HF-cleaned SOS substrates. The basic growth process is similar to that described in the preceding section, except that the intermediate STO buffer layers were typically grown at a 120 mT oxygen pressure at nominal temperatures approximately 40° below the YSZ and YBCO growth temperature. Typical layer thicknesses were: YBCO - 1200-1500Å; STO - 1600-2000Å; and YSZ - 500-800Å.

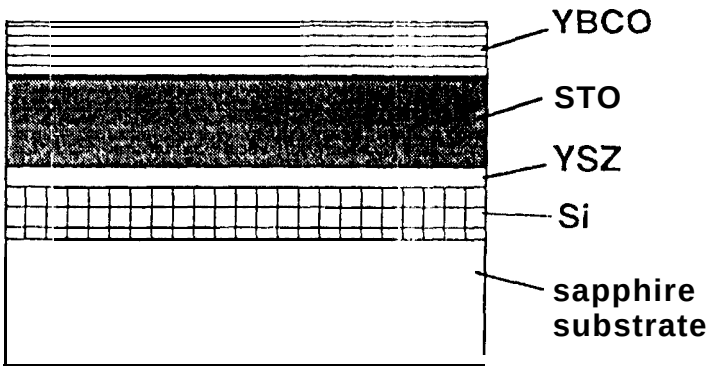

Figure 3. Schematic cross-section of YBCO/$SrTiO_3$/YSZ/SOS heterostructure. Structural studies indicate that the STO layer does not grow epitaxially over YSZ.

The YBCO/$SrTiO_3$/YSZ/SOS multilayer structures were studied using x-ray diffraction, cross-sectional HRTEM, and ac susceptibility. All of these methods indicated that the STO did not grow epitaxially on the underlying YSZ buffer layer, which resulted in a very poor quality YBCO top layer. X-ray diffraction measurements on the sample displayed only diffraction peaks from the sapphire substrate and the Si and YSZ epilayers: there were no YBCO or STO diffraction peaks. The HRTEM cross-sections confirmed the x-ray analysis: the lattice images and electron diffraction patterns showed crystalline Si and YSZ epilayers, but there was no clear boundary between the STO and YBCO layers, and no long-range crystallinity in those layers. AC susceptibility measurements of the YBCO film on

the same sample showed no superconducting transition to below 10 K. All of these results are consistent with very poor quality STO growth on the YSZ buffer layer, which is supported by a previous study of epitaxial insulator multilayer growth[25]. The reason that STO does not grow epitaxially on ZrO_2 (100) surfaces may be qualitatively understood by considering the (100) surface terminations of the two materials. In the [100] direction, cubic ZrO_2 consists of alternating anion and cation planes, while $SrTiO_3$ consists of alternating Sr-O and $Ti-O_2$ (i.e. mixed anion-cation) layers. An epitaxial interface would thus require ions of the same charge to be in close proximity, which is energetically unfavorable.

4.2 YBCO/$SrTiO_3$/YBCO/YSZ/SOS heterostructures

Although STO does not grow epitaxially on YSZ buffer ***layers,*** a relatively simple modification of the structure shown in Figure 3 produces a dramatic improvement in the epitaxial quality of the STO and YBCO overlayers. This modification is based upon the observations that YBCO (and analogs, such as PBCO) exhibit high quality epitaxial growth on YSZ, and STO is known to grow epitaxially over YBCO epilayers. Hence the addition of a thin YBCO (or PBCO) "seed layer" over the YSZ buffer on the SOS substrate should serve as a growth template for epitaxy of the STO and YBCO overlayers. The basic idea is illustrated in Figure 4. We have produced heterostructures of this type, and do, in fact, see a remarkable improvement in the STO and YBCO film quality relative to structures without the seed layer, as determined by x-ray diffraction, ac susceptibility, and HRTEM measurements.

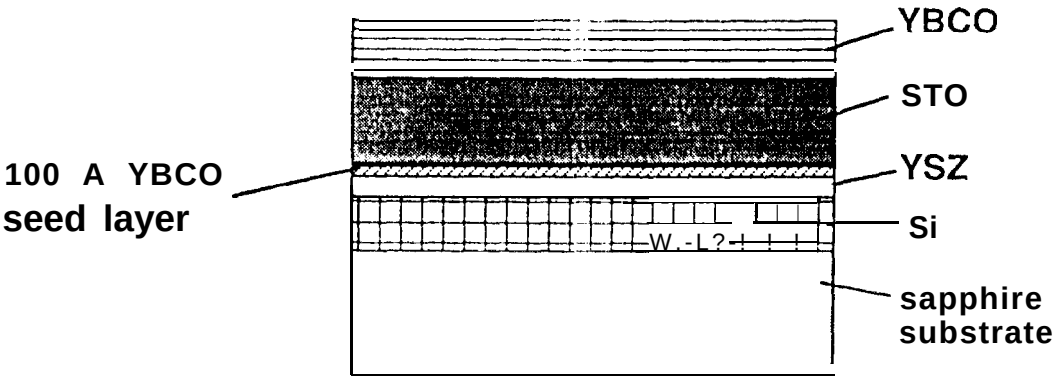

Figure 4. Schematic cross-section of YBCO/$SrTiO_3$/YBCO/YSZ/SOS heterostructure. The addition of a thin YBCO (or PBCO) seed layer results in a dramatic improvement in the epitaxial quality of the STO and YBCO overlayers.

The basic film growth process and layer thicknesses for the structure shown in Figure 4 are the same as the process described in the previous sections, except that a thin (100-200~) YBCO film is grown using our standard YBCO deposition process just before growth of the STO. X-ray θ--2θ scans of multilayers produced in this way show all the expected S1'0 and YBCO(00*l*) diffraction peaks, indicating that the STO and YBCO layers are epitaxial, unlike structures without the YBCO seed layer. In addition, ac susceptibility measurements show a dramatic improvement in the superconducting properties of the YBCO top layer: ac susceptibility data for a YBCO/STO/YBCO/YSZ/SOS heterostructure with a 100 Å YBCO seed layer shows a sharp superconducting transition with an onset at 89.6 K and a transition width of 0.6 K. This result is comparable to our best films on $LaAlO_3$ and should be contrasted to the same measurements made on structures without the YBCO seed layer, which were not superconducting to below 10 K. Using a cleavage technique for sample preparation, cross-sectional HRTEM studies were also done on these samples. Figure 5 shows a TEM cross-section of a YBCO/STO/YBCO/YSZ/SOS heterostructure and convergent-beam-electron-diffraction patterns for each layer except the thin YBCO seed layer. The magnified views of the YBCO seed layer and the

YBCO top layer show that the YBCO films arc epitax[illegible]ented The bottom of he YBCO seed layer also shows the expected $BaZrO_3$ reaction [illegible]YBCO-YSZ interface. Although difficult to see on the scale of the figure, clean lattice[illegible]present for the Si, YSZ, and STO layers, and the electron diffraction patterns confirm t hat [illegible]epitaxial

The x-ray, ac susceptibility, and HRTEM studies[illegible]incorporation of the YBCO seed layer leads to a great improvement in the epitaxial qua[illegible]of the STO and YBCO overlayers. While this scheme is somewhat complicated, it does work well. and[illegible]has the advantage that a superconducting ground plane can be naturally incorporated into the device structure. simply by using a thicker YBCO seed layer. More quantitative studies of the epitaxial quality and the transport properties of the top YBCO layer arc in progress, and will be reported on c[illegible]ter.

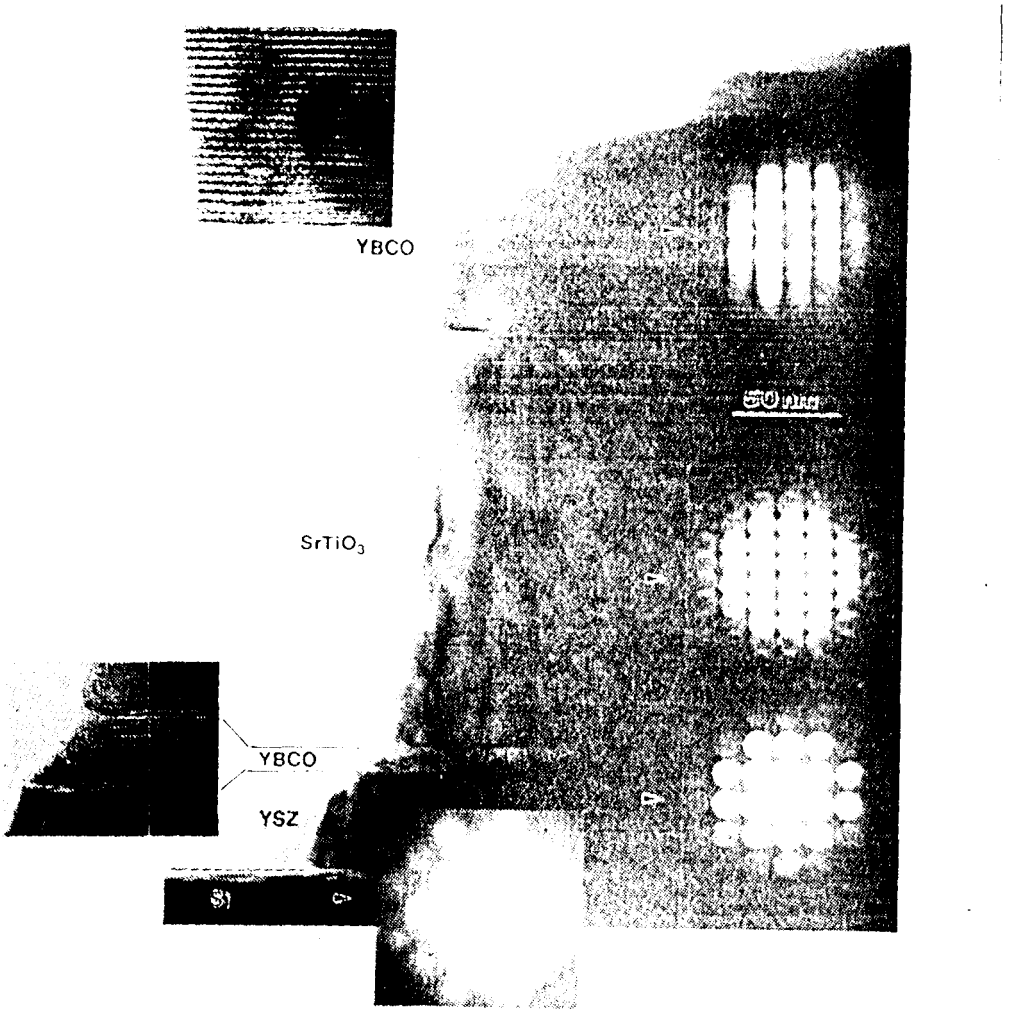

Figure 5. Cross-sectional I-EM micrograph of YBCO/[illegible]YBCO/YSZ/SOS heterostructure with convergent-beam diffraction patterns from each layer. Interference fringes and diffraction patterns indicate that all layers are epitaxial, in contrast to heterostructures which do not include the thin YBCO seed layer.

4.3 SNS weak link fabrication using YBCO/STO/YBCO/YSZ/SOS heterostructures

Edge-geometry SNS weak links have been fabricated using the STO/YBCO/YSZ multilayer buffer system on SOS substrates. The structure shown in Figure 4 serves as the starting point for device fabrication, with the top YBCO film becoming the base electrode of the completed SNS edge junction. We used our standard edge-geometry weak link process for device fabrication, with base electrode YBCO thicknesses of= 1200 Å, PBCO normal metal thicknesses of 65-150 Å, and counterelectrode thicknesses of 1100-1500 Å. The current-voltage characteristics for a YBCO/PBCO/YBCO edge-geometry weak link on the multilayer buffer system on a silicon-on-sapphire substrate are shown in Figure 6. The PBCO thickness is 65 Å anti the temperature is 65 K. The electrical characteristics are qualitatively consistent with the resistively-shunted junction (RSJ) model, although there is a significant amount of excess current. The weak link critical current density is approximately 2 x 10^4 A/cm^2 and the I_cR_n product is 145 μV, which arc reasonable values for this operating temperature and PBCO thickness.

The I-V data in Figure 6 shows no evidence for the series weak links that were seen in edge junctions fabricated directly on YSZ buffer layers (Figure 2). This demonstrates that the multilayer STO/YBCO/YSZ buffer system is preventing grain-boundary nucleation at the base-electrode YBCO/insulator interface. At higher drive currents and voltages (greater than several mA and mV), the device shown in Figure 6 does exhibit a gradual transition to higher resistance, which probably indicates that the counterelectrode critical current density is somewhat reduced and further optimization of the process is needed. Nonetheless, the electrical characteristics show that the addition of the YBCO seed layer and thicker STO buffer layer above the YSZ buffer enables the fabrication of high quality edge-geometry SNS weak links on silicon-on-sapphire substrates. This development provides the technology necessary for ultra-high frequency HTS superconducting device applications, as well as enabling the integration of superconductor and semiconductor circuitry.

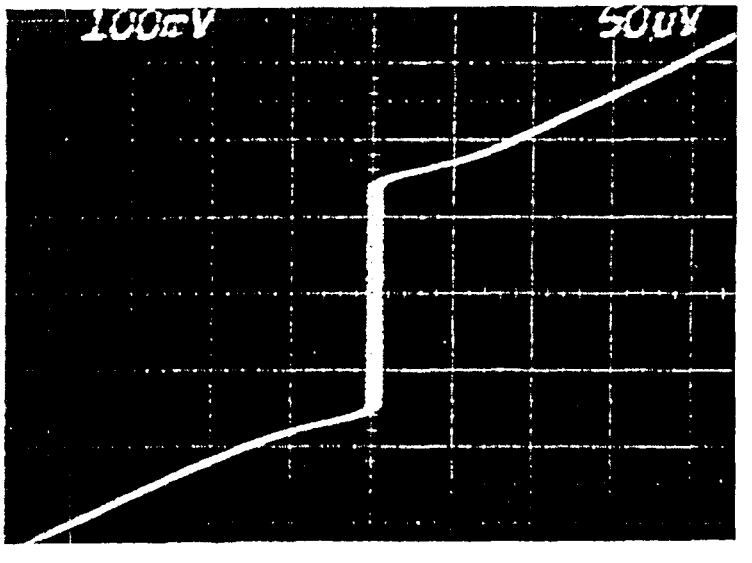

Figure 6. I-V characteristics for a YBCO edge-geometry weak link on a STO/YBCO/YSZ multilayer buffer on an SOS substrate with a 65 Å PBCO normal metal layer at 65 K. The counterelectrode is 2.5 μm wide, and the base electrode is 1230 Å thick. The electrical characteristics show no evidence for a series grain-boundary weak link. The vertical scale is 100 μA/div. and the horizontal scale is 50 μV/div.

5. SUMMARY

We have developed a multilayer buffer system which enables the fabrication of high-quality, epitaxial, edge-geometry SNS weak links on silicon-on-sapphire substrates. The buffer layer system consists of an epitaxial STO/seed-YBCO/YSZ multilayer heterostructure grown on an HF-cleaned SOS substrate. The novel feature of this approach is the incorporation of the thin YBCO seed layer which serves as a template for growth of a high quality STO overlayer. YBCO/STO/YBCO/YSZ/SOS heterostructures show a dramatic improvement in S1'0 and YBCO film quality relative to structures which do not incorporate the YBCO seed layer, Without the multilayer buffer system, devices fabricated directly on single YSZ buffer layers exhibit problems with grain boundary nucleation at the base-YBCO/YSZ interface. However, SNS junctions fabricated on STO/YBCO/YSZ buffers have greatly improved electrical characteristics, with RSJ-like I-V characteristics, and no evidence for series grain boundary weak links. This is the first demonstration of high-quality, epitaxial, edge-geometry SNS weak links on SOS substrates, and provides a key technology necessary for ultra-high frequency HTS superconducting device applications, as well as for integration of superconductor and semiconductor circuitry.

6. ACKNOWLEDGEMENTS

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